CENG 215 Circuits and Electronics

LAB #4 Feuille

Place: PC Lab

Aim

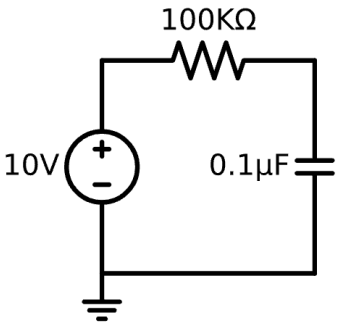
To build and analyze various resistive networks in PySpice and to compare the analysis results with the theoretical analysis results.

Materials/Devices:

PySpice

Work to be done:

The following circuit is a first order R-C circuit. Assume that the capacitor is initially discharged and 10V voltage source is applied at time zero.



1. Simulate the circuit and plot the capacitor voltage $V_c(t)$.
    a. Try these voltage sources and discuss the results:
        i. `source = circuit.VoltageSource('input', 'in', circuit.gnd, 10@u_V)`
        ii. `source = circuit.PieceWiseLinearVoltageSource('input', 'in', circuit.gnd, values=[(0,0),(0,10@u_V)])`
        iii. `source = circuit.PulseVoltageSource('input', 'in', circuit.gnd, initial_value=0@u_V, pulsed_value=10@u_V,pulse_width=100@u_ms, period=200@u_ms)`
    b. What is V_c at t=20μs ? Find it both theoretically and by simulation.
    c. In transient simulation, change the “step_time” parameter and observe its effect.

Final Remarks