CENG 215 Circuits and Electronics

LAB #5 Feuille

Place: PC Lab

Aim

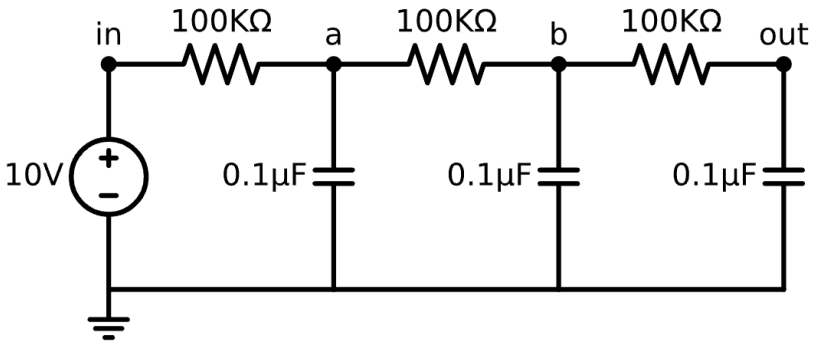
To build and analyze various resistive networks in PySpice and to compare the analysis results with the theoretical analysis results.

Materials/Devices:

PySpice

Work to be done:

Consider the following circuit that consists of resistors and capacitors. Assume that the capacitors are initially discharged and 10V voltage source is applied at time zero.



1. Simulate the circuit and plot the following signals:
    a. $V_{in}(t)$
    b. $V_a(t)$
    c. $V_b(t)$
    d. $V_{out}(t)$

2. Which signals seem to be in exponential shape? Discuss.

3. Show numerically whether $V_a(t)$ is exponential or not. (HINT: You can try to fit an exponential curve to $V_a(t)$ data. If there is a good fit then you can conclude that the signal is exponential)

Final Remarks

-